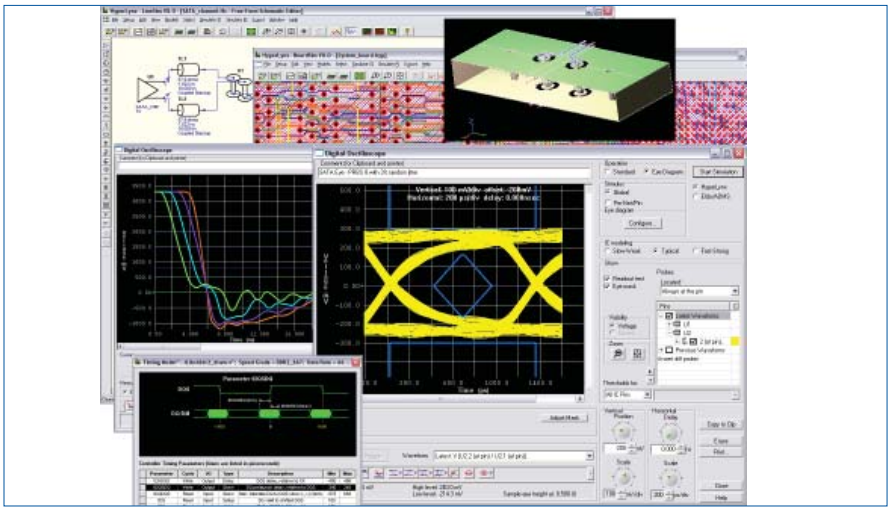
HyperLynx SI



HyperLynx SI includes tools for pre- and post-layout signal integrity, timing, crosstalk, and EMC analysis, for signals ranging from 0 Hz to multi-GHz.

Overview

Signal integrity (SI) analysis is an essential part of modern electronic design. Increasingly fast edge rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies. As driver ICs switch faster, a growing volume of boards suffer from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail.

Hardware engineers, PCB designers and signal integrity specialists alike can use HyperLynx as a team; getting simulation results without requiring weeks of software training. The emphasis is on getting designs right the first time, avoiding costly overdesign, and saving recurrent layout, prototype and test cycles in the lab.

Complete SI and EMC Analysis Suite

With HyperLynx, you can address high-speed PCB problems throughout the design cycle, beginning at the earliest architectural stages and moving through post-layout verification. The process is as easy as using an oscilloscope or spectrum analyzer in the lab, and at a fraction of the cost.

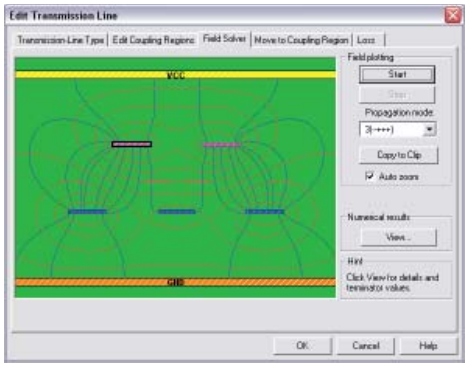
MAJOR BENEFITS:

- Industry-renowned ease of use, enabling shorter time to results
- Accurate modeling of trace impedance, coupling, and frequency-dependent losses
- Sweep different values for discretes, trace geometries and lengths, and driver settings
- Terminator Wizard™ recommends optimal termination strategies
- Integrated timing analysis for DDR, DDR2, and DDR3
- Industry-leading SERDES support including fast eye diagram analysis, S-parameter simulation, and BER prediction
- Advanced, exploratory via modeling
- Integrated full-wave 3D electromagnetic field solver
- Provides an early look at likely EMC failures
- Integration with the constraint editing system (CES)
- Works with all major PCB layout and routing applications

Pre-layout analysis

Pre-layout simulation allows you to predict and eliminate signal integrity problems early, allowing proactive con-strain routing, planning stackups, and optimizing clock, critical signal topologies and terminations prior to layout. The intuitive drag-and-drop transmission-line modeling is an ideal way to get your design right the first time.

- Quickly enter complex interconnects, including ICs, traces, vias, cables, connectors and passive components.
- Integrated 2D and 3D field solvers for accurate modeling and solution space exploration.
- Simulate immediately, using industry-standard IBIS Models (a library is included), generic models, or build your own models from databook information.
- Visual IBIS Editor allows you to check/edit IBIS models including a heirarchical, automated syntax.
- Easily instantiate HSPICE, ELDO, IBIS-AMI, AMS, S-parameter, and IBIS models.
- Start from scratch or use our many design kits for technologies likes PCI Express, DDR2, and PCI-X, or one of our many FPGA design kits.
- Accurately predict serial interface bit error rates (BER), worst-case bit sequences, and eye diagrams in hours instead of weeks using HyperLynx FastEye™.
- Wizard-guided full design exploration for DDRx designs in a pre-layout environment



Pre-layout crosstalk analysis allows you to optimize spacing, stackup, and termination.

Post-layout verification

Post-layout SI simulation allows you to analyze signal integrity and timing at three important stages: following part placement in your PCB layout system, after critical net routing, and after detailed routing of an entire board.

- Batch simulation automatically scans large numbers of nets on an entire PCB, flagging SI and EMC hot spots
- Interactive analysis takes you to the next level, simulating batch analysis-identified trouble spots
- Quick Terminators allow new termination components to be inserted on-the-fly, enabling real-time analysis
- Accurately predicts crosstalk waveforms for any trace topology and IC placement, showing board designers specific cross-sections violating crosstalk thresholds
- Powerful, easy to use multi-board analysis, including support for EBD models and connector models
- DDRx wizard allows complete verification of DDR, DDR2, and DDR3 memory systems, including timing
- Interface to full-wave 3D field solver allows for extraction and analysis of complex layout structures, such as coupled via fields, breakouts, and plane gaps.

Supported PCB layout systems:

- Mentor Graphics PADS® Layout, Expedition™ PCB and Board Station®
- Cadence Allegro and OrCAD Layout
- Altium Protel and P-CAD
- Intercept Pantheon
- Zuken CADStar, Visula and CR3000/5000 PWS or Board Designer

Platforms Supported

- 32-bit Windows 7/Vista/XP/Server2003/2008
- 64-bit Windows 7/Vista/Server2003/2008
- 32- and 64-bit Linux RHEL 4/5 and SLES 10
- Solaris 10

For the latest product information, call us or visit: www.mentor.com/hyperlynx

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

MF 1-13 1030050-w