

Single P-Channel MOSFET

DESCRIPTION

SMC4427 is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior ,fast switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

PART NUMBER INFORMATION

SMC 4427 M - TR G
 a b c d e

- a : Company name.
- b : Product Serial number.
- c : Package code M:SOP-8
- d : Handling code TR:Tape&Reel
- e : Green produce code G:RoHS Compliant

FEATURES

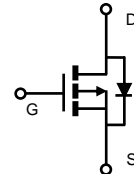
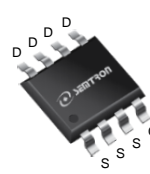
$V_{DS} = -30V$, $I_D = -15A$

$R_{DS(ON)} = 7.5m\Omega(Typ.) @ V_{GS} = -10V$
 $R_{DS(ON)} = 11.5m\Omega(Typ.) @ V_{GS} = -4.5V$

- ◆ Fast switch
- ◆ High power and current handling capability

APPLICATIONS

- ◆ Load Switch
- ◆ LED Application
- ◆ DC-DC Power Management



SOP-8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	-15
		$T_A = 70^\circ C$	-12
I_{DM}	Pulsed Drain Current ^A	-60	A
I_{AS}	Avalanche Current ^A	-30	A
E_{AS}	Single Pulse Avalanche energy $L=0.1mH$ ^{AE}	45	mJ
P_D	Power Dissipation ^B	$T_A = 25^\circ C$	3.1
		$T_A = 70^\circ C$	2
T_J	Operation Junction Temperature	-55/150	$^\circ C$
T_{STG}	Storage Temperature Range	-55/150	$^\circ C$

THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^B	$t \leq 10s$	40	$^\circ C/W$
	Thermal Resistance Junction to Ambient ^{BC}	Steady-State	75	
$R_{\theta JC}$	Thermal Resistance Junction to Case		25	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

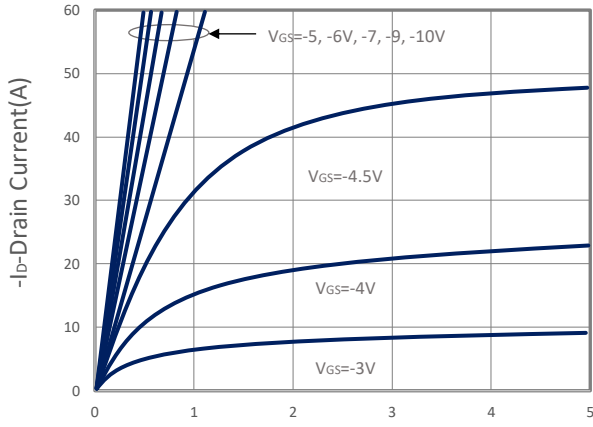
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μ A	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μ A	-1	-1.6	-2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = \pm 20V			\pm 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =25 $^\circ$ C			-1	μ A
		V _{DS} =-24V, V _{GS} =0V, T _J =75 $^\circ$ C			-10	
R _{DS(ON)}	Drain-source On-Resistance ^D	V _{GS} =-10V, I _D =-15A V _{GS} =-4.5V, I _D =-10A		7.5 11.5	9 14	m Ω
G _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-10A		14.8		S
Diode Characteristics						
V _{SD}	Diode Forward Voltage ^D	I _S =-1A, V _{GS} =0V			-1	V
I _S	Continuous Source Current				-7.5	A
t _{rr}	Reverse Recovery Time	I _S =-10A, dI/dt=100A/ μ s		21		ns
Q _{rr}	Reverse Recovery Charge			15.5		nC
Dynamic and Switching Parameters						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V I _D =-10A		61	85	nC
Q _g	Total Gate Charge (4.5V)			30	42	
Q _{gs}	Gate-Source Charge			10.6	14.8	
Q _{gd}	Gate-Drain Charge			9	12.6	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		3230		pF
C _{oss}	Output Capacitance			369		
C _{rss}	Reverse Transfer Capacitance			265		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		8.3		Ω
t _{d(on)}	Turn-On Time ^D	V _{DD} =-15V, V _{GEN} =-10V R _G =3 Ω , I _D =-1A		24	46	nS
t _r				11.6	22	
t _{d(off)}	Turn-Off Time ^D			78.8	150	
t _f				33.4	63	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

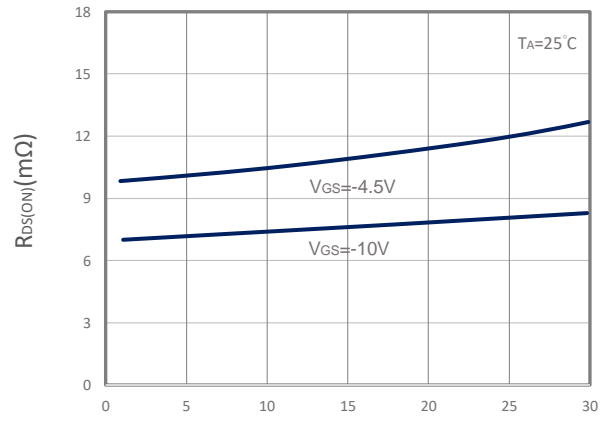
- A. Pulsed width limited by maximum junction temperature, T_{J(MAX)}=150 $^\circ$ C.
- B. Measure the value in a still air environment at T_A=25 $^\circ$ C, using an installation mounted on a 1 in2 FR-4 board, maximum junction temperature T_{J(MAX)}=150 $^\circ$ C.
- C. T_{J(MAX)}=150 $^\circ$ C, using junction-to-case thermal resistance (R_{θJC}) is more useful in additional heat sinking is used.
- D. The pulse test width is \leq 300 μ s and the duty cycle \leq 2%.
- E. The EAS data shows Maximum, tested and pulse width limited by maximum.

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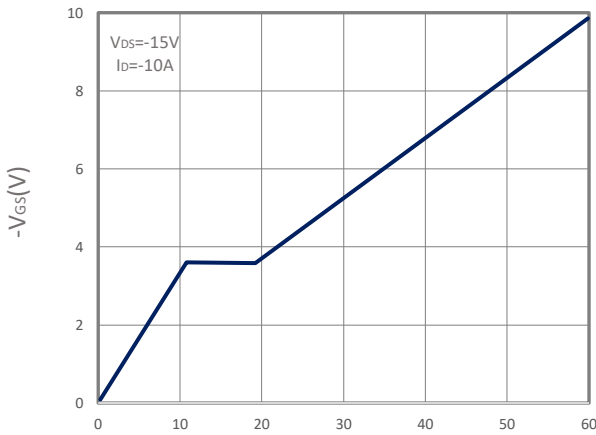
TYPICAL CHARACTERISTICS



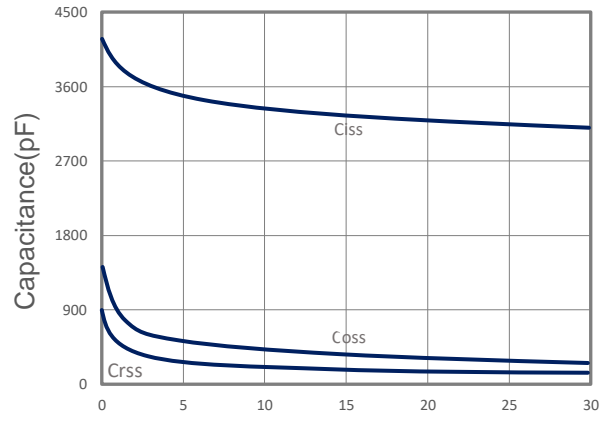
Output Characteristics



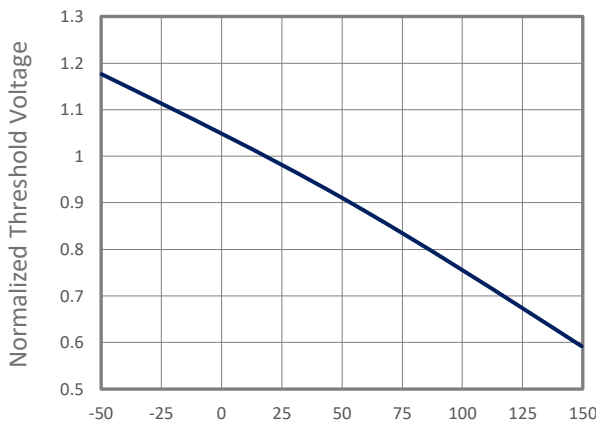
Drain-Source On Resistance



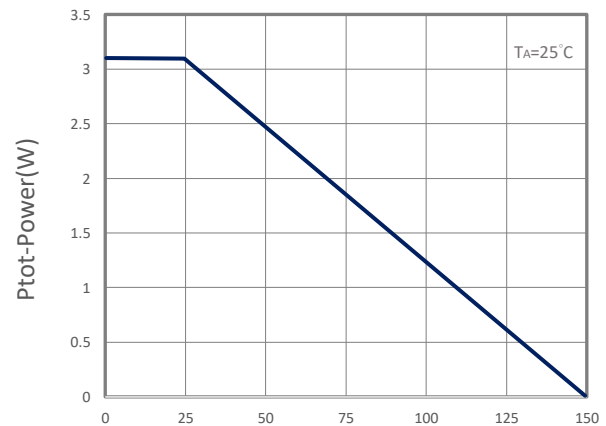
Gate Charge



Capacitance

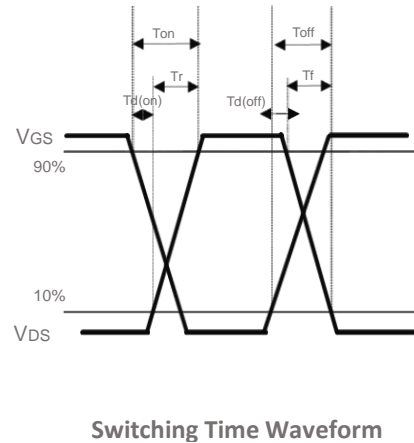
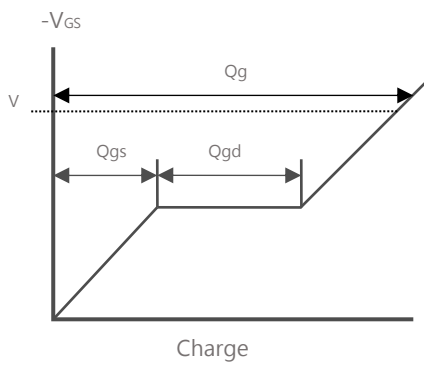
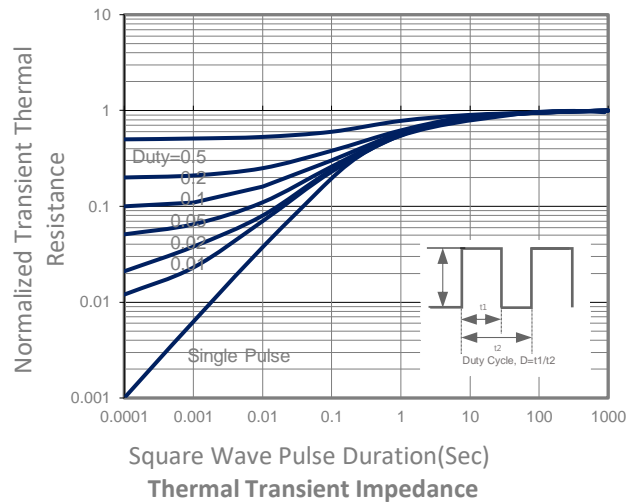
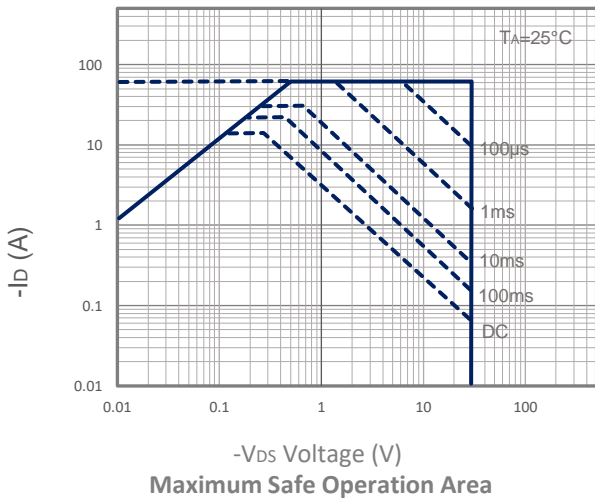
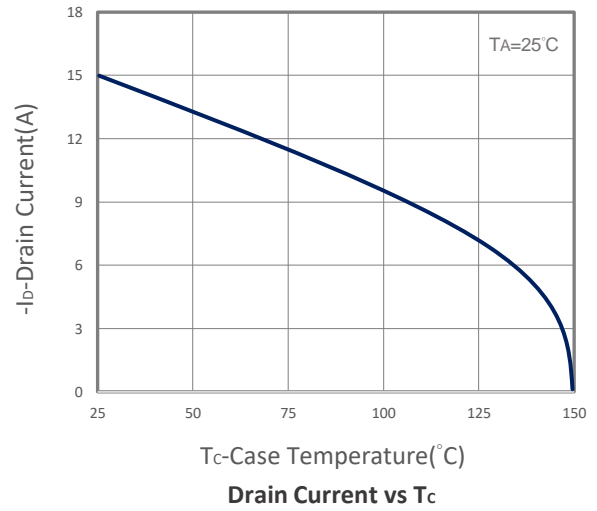
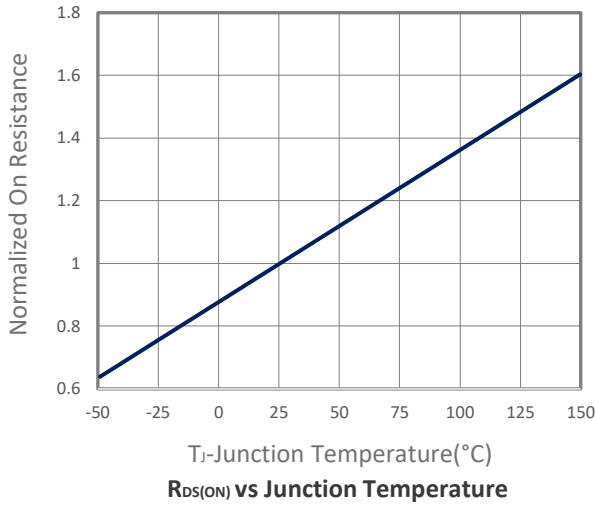


Gate Threshold Voltage

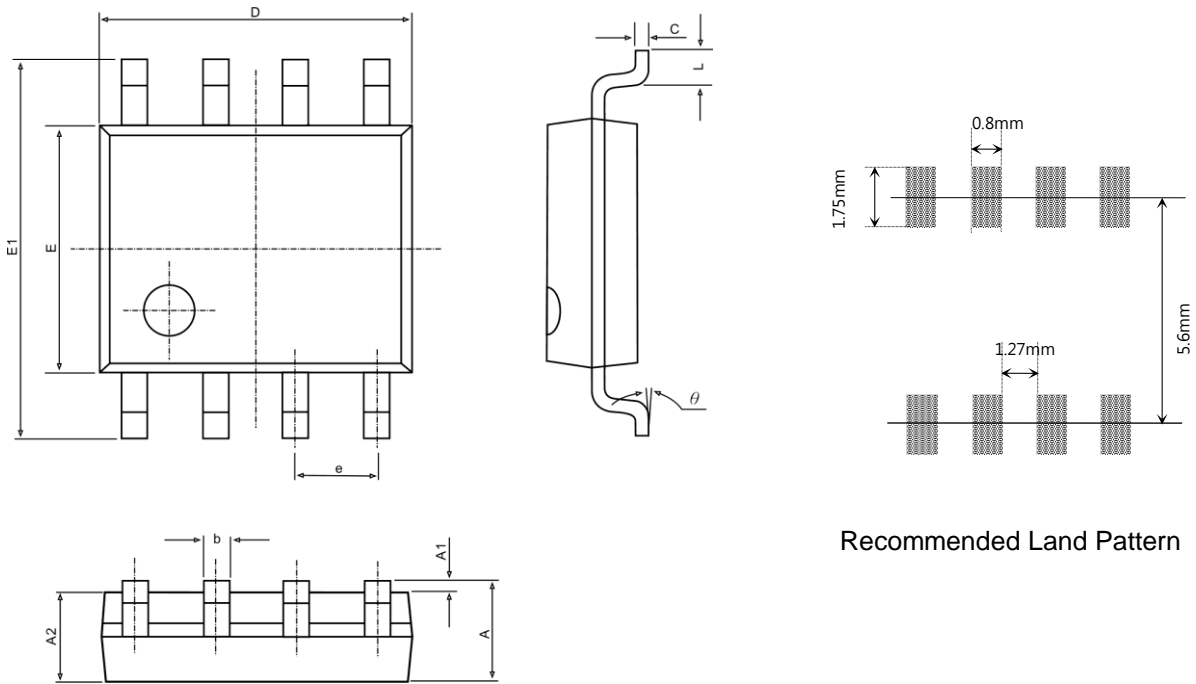


Power Dissipation

TYPICAL CHARACTERISTICS



■ SOP-8 PACKAGE DIMENSIONS



Recommended Land Pattern

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.130	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270BSC.		0.050BSC.	
L	0.400	1.270	0.016	0.005
θ	0°	8°	0°	8°